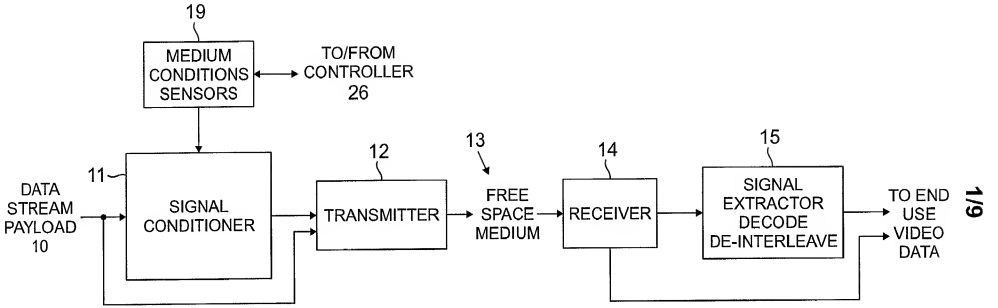


FIG. 1

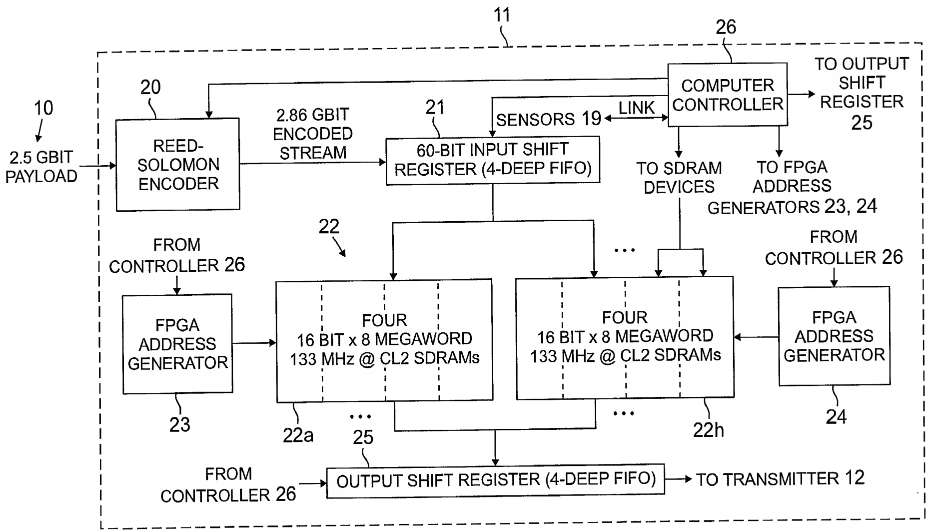
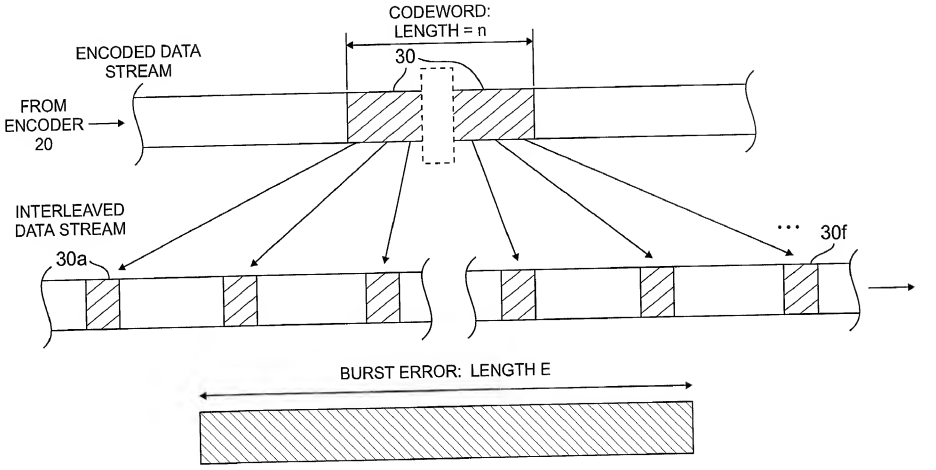

11
10
2.5 GBIT
PAYLOAD
20
REED-
SOLOMON
ENCODER
2.86 GBIT
ENCODED
STREAM
21
60-BIT INPUT SHIFT
REGISTER (4-DEEP FIFO)
SENSORS 19
LINK
26
COMPUTER
CONTROLLER
TO OUTPUT
SHIFT
REGISTER
25
TO SDRAM
DEVICES
TO FPGA
ADDRESS
GENERATORS 23, 24
22
FROM
CONTROLLER 26
FPGA
ADDRESS
GENERATOR
23
FOUR
16 BIT x 8 MEGAWORD
133 MHz @ CL2 SDRAMs
22a
FOUR
16 BIT x 8 MEGAWORD
133 MHz @ CL2 SDRAMs
22h
FROM
CONTROLLER 26
FPGA
ADDRESS
GENERATOR
24
25
FROM
CONTROLLER 26
OUTPUT SHIFT REGISTER (4-DEEP FIFO)
TO TRANSMITTER 12

FIG. 2



INTERLEAVING THE ENCODED PAYLOAD

FIG. 3

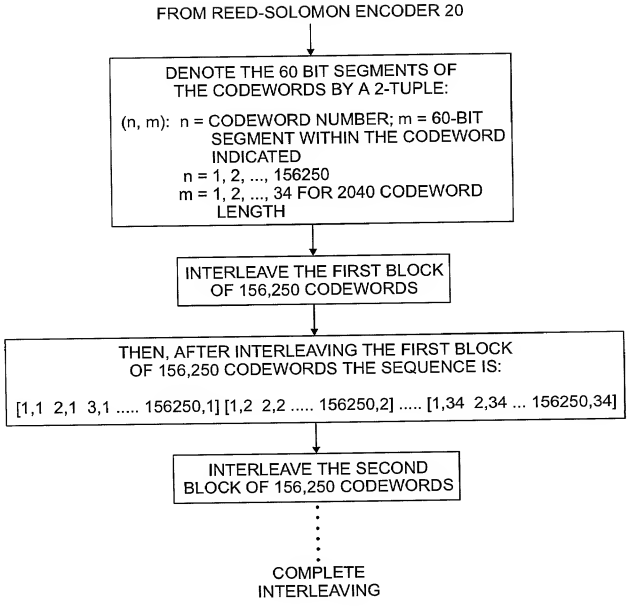

FROM REED-SOLOMON ENCODER 20
DENOTE THE 60 BIT SEGMENTS OF THE CODEWORDS BY A 2-TUPLE:
(n, m): n = CODEWORD NUMBER; m = 60-BIT SEGMENT WITHIN THE CODEWORD INDICATED
n = 1, 2, ..., 156250
m = 1, 2, ..., 34 FOR 2040 CODEWORD LENGTH
INTERLEAVE THE FIRST BLOCK OF 156,250 CODEWORDS
THEN, AFTER INTERLEAVING THE FIRST BLOCK OF 156,250 CODEWORDS THE SEQUENCE IS:
[1,1 2,1 3,1 ..... 156250,1] [1,2 2,2 ..... 156250,2] ..... [1,34 2,34 ... 156250,34]
INTERLEAVE THE SECOND BLOCK OF 156,250 CODEWORDS
COMPLETE INTERLEAVING

FIG. 4

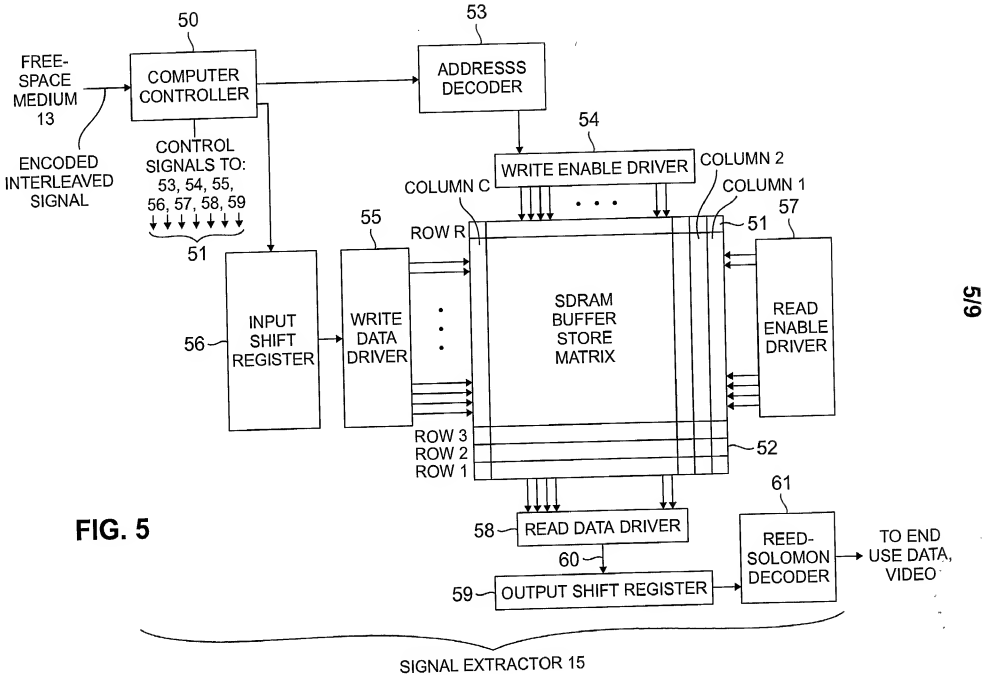
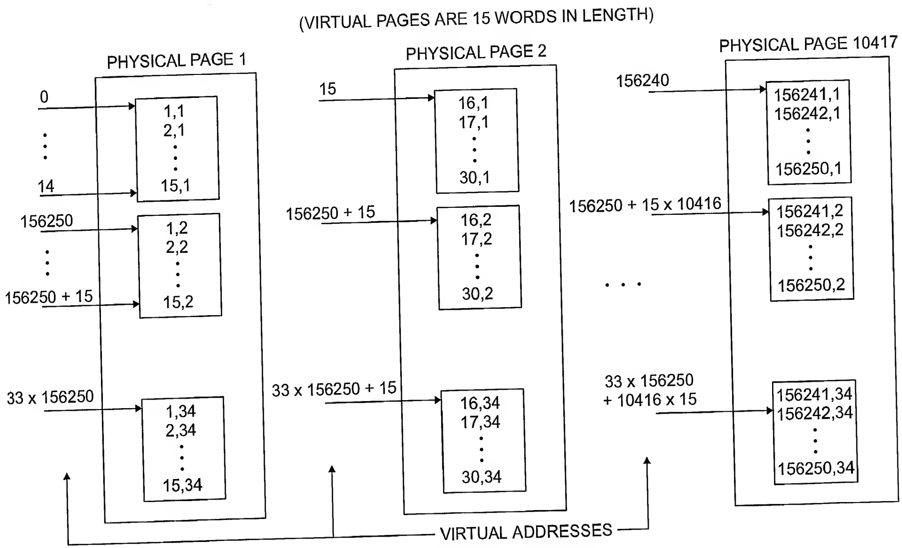

50
53
FREE-SPACE MEDIUM 13
COMPUTER CONTROLLER
ADDRESSS DECODER
ENCODED INTERLEAVED SIGNAL
CONTROL SIGNALS TO: 53, 54, 55, 56, 57, 58, 59
51
54
WRITE ENABLE DRIVER
COLUMN 2
COLUMN C
COLUMN 1
55
ROW R
51
57
INPUT SHIFT REGISTER
56
WRITE DATA DRIVER
SDRAM BUFFER STORE MATRIX
READ ENABLE DRIVER
ROW 3
ROW 2
ROW 1
52
61
58
READ DATA DRIVER
REED-SOLOMON DECODER
TO END USE DATA, VIDEO
60
59
OUTPUT SHIFT REGISTER
SIGNAL EXTRACTOR 15

FIG. 5



REMAPPING ADDRESSES TO BALANCE "READ" VS. "WRITE" OVERHEAD IN TERMS OF SDRAM PAGE CHANGES

FIG. 6A

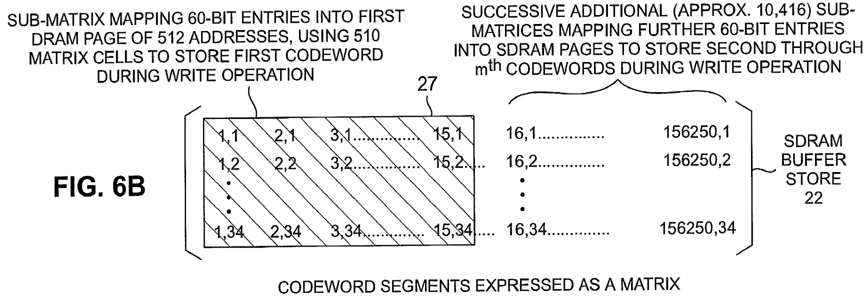

SUB-MATRIX MAPPING 60-BIT ENTRIES INTO FIRST DRAM PAGE OF 512 ADDRESSES, USING 510 MATRIX CELLS TO STORE FIRST CODEWORD DURING WRITE OPERATION
27
SUCCESSIVE ADDITIONAL (APPROX. 10,416) SUB-MATRICES MAPPING FURTHER 60-BIT ENTRIES INTO SDRAM PAGES TO STORE SECOND THROUGH mth CODEWORDS DURING WRITE OPERATION
1,1 2,1 3,1.............. 15,1 16,1.............. 156250,1
1,2 2,2 3,2.............. 15,2.... 16,2.............. 156250,2
1,34 2,34 3,34.............. 15,34.... 16,34.............. 156250,34
SDRAM BUFFER STORE 22
CODEWORD SEGMENTS EXPRESSED AS A MATRIX

FIG. 6B

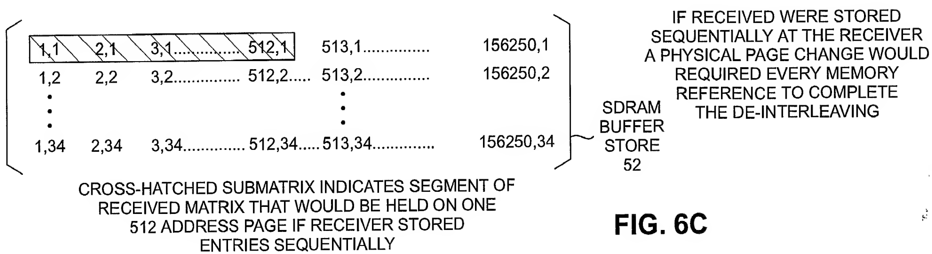

1,1 2,1 3,1.............. 512,1 513,1.............. 156250,1
1,2 2,2 3,2.............. 512,2..... 513,2.............. 156250,2
1,34 2,34 3,34.............. 512,34..... 513,34.............. 156250,34
SDRAM BUFFER STORE 52
IF RECEIVED WERE STORED SEQUENTIALLY AT THE RECEIVER A PHYSICAL PAGE CHANGE WOULD REQUIRED EVERY MEMORY REFERENCE TO COMPLETE THE DE-INTERLEAVING
CROSS-HATCHED SUBMATRIX INDICATES SEGMENT OF RECEIVED MATRIX THAT WOULD BE HELD ON ONE 512 ADDRESS PAGE IF RECEIVER STORED ENTRIES SEQUENTIALLY

FIG. 6C

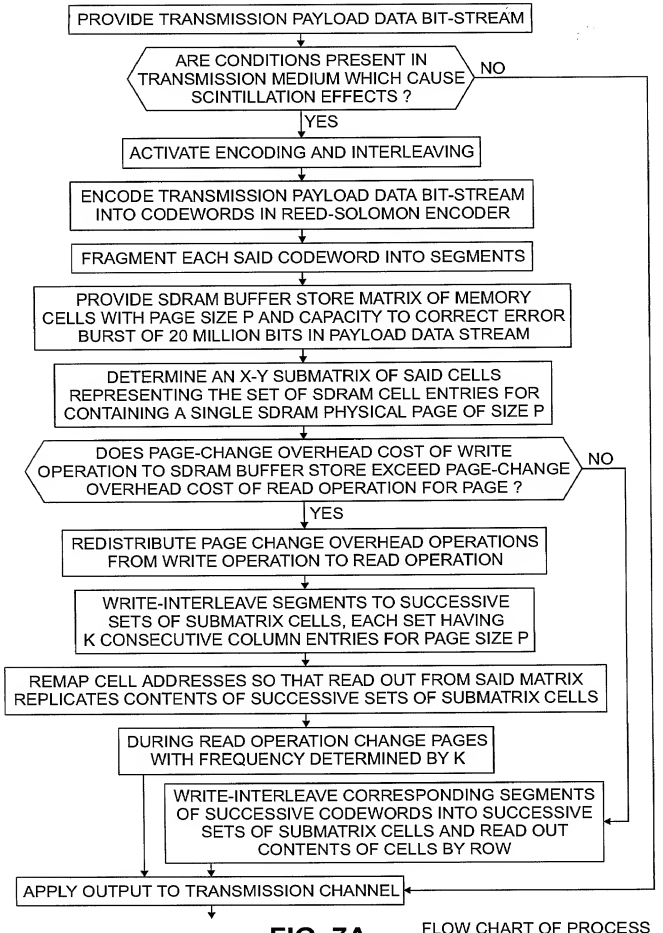
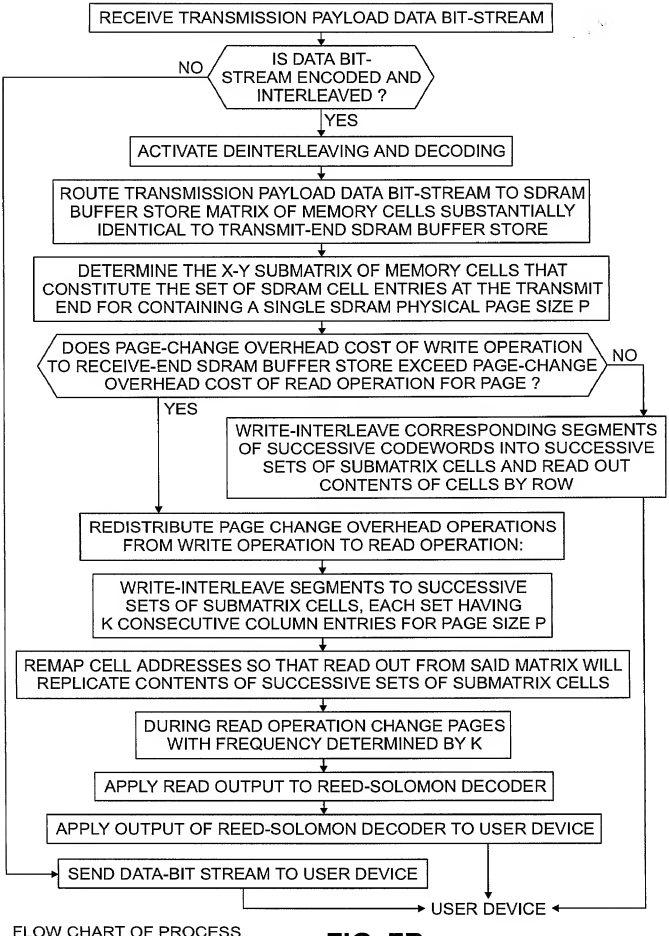


FIG. 7A FLOW CHART OF PROCESS AT TRANSMITTER END



FLOW CHART OF PROCESS AT RECEIVER END

FIG. 7B